AMENDMENTS TO THE SPECIFICATION

Please add the following paragraph after paragraph [0051]

Figure 20 is a flowchart illustrating operation of the microprocessor of Figure 3 to predict return instruction addresses according to the present invention.

Please add the following paragraphs after paragraph [0231]:

Referring now to Figure 20, a flowchart illustrating operation of the microprocessor 300 of Figure 3 to predict return instruction addresses according to the present invention is shown. Flow begins at block 2002.

At block 2002, as a cache line is being fetched from the instruction cache 432 at the fetch address 495, the fetch address 495 also indexes the BTAC 402, as described above with respect to Figure 4. The BTAC 402 predicts the cache line contains a first CALL instruction via the SBI 454, as described above with respect to Figure 4 and decision blocks 1302 and 1304 of Figure 13. Flow proceeds to block 2004.

At block 2004, in response to the BTAC 402 predicting the first CALL instruction, the adder 434 calculates the return address 491 of the first CALL instruction, as discussed above with respect to Figure 4, which is pushed onto the speculative CALL/RET stack 406, as discussed above with respect to block 1306 of Figure 13. Flow proceeds to block 2006.

At block 2006, as a subsequent cache line is being fetched from the instruction cache 432, the BTAC 402 predicts the cache line contains a second CALL instruction. Flow proceeds to block 2008.

At block 2008, in response to the BTAC 402 predicting the second CALL instruction, the adder 434 calculates the return address 491 of the second CALL instruction, which is pushed onto the speculative CALL/RET stack 406. Flow proceeds to block 2012.

At block 2012, as a subsequent cache line is being fetched from the instruction cache 432, the BTAC 402 predicts the cache line contains a first RET instruction via the SBI

454, as described above with respect to Figure 4 and decision blocks 1302 and 1312 of Figure 13. Flow proceeds to block 2014.

At block 2014, in response to the BTAC 402 predicting the first RET instruction, the speculative CALL/RET stack 406 pops a return address 353, which is the second CALL instruction return address that was pushed at block 2008, according to block 1314 of Figure 13, and the control logic 404 controls mux 422 to select the popped return address 353 for provision as the current fetch address 495 to the instruction cache 432 to cause fetching to branch to the popped return address 353, as described above with respect to Figure 4 and block 1316 of Figure 13. Flow proceeds to block 2016.

At block 2016, as a subsequent cache line is being fetched from the instruction cache 432, the BTAC 402 predicts the cache line contains a second RET instruction. Flow proceeds to block 2018.

At block 2018, in response to the BTAC 402 predicting the second RET instruction, the speculative CALL/RET stack 406 pops the first CALL instruction return address that was pushed at block 2004 and the control logic 404 branches to the popped return address 353. Flow proceeds to block 2022.

At block 2022, the first CALL instruction reaches the instruction decode logic 436 which decodes it and calculates the return address 488 of the first CALL instruction, which is pushed onto the non-speculative CALL/RET stack 414, as discussed above with respect to Figure 4. Flow proceeds to block 2024.

At block 2024, the second CALL instruction reaches the instruction decode logic 436 which decodes it and calculates the return address 488 of the second CALL instruction, which is pushed onto the non-speculative CALL/RET stack 414. Flow proceeds to block 2026.

At block 2026, the first RET instruction reaches the instruction decode logic 436 which decodes it and indicates the presence of the first RET instruction to the non-speculative CALL/RET stack 414 via instruction decode information 492, as described above with respect to Figure 4. In response, non-speculative CALL/RET stack 414 pops the return

address 355 of the second CALL instruction, which was pushed onto the non-speculative CALL/RET stack 414 at block 2024. Flow proceeds to block 2028.

At block 2028, the comparator 418 compares the return address 353 provided by the speculative CALL/RET stack 406 at block 2014 with the return address 355 provided by the non-speculative CALL/RET stack 414 at block 2026, as described above with respect to Figure 4 and block 1318 of Figure 13. Flow proceeds to decision block 2032.

At decision block 2032, the control logic 404 receives the result 474 of the comparison made by the comparator 418 at block 2028 to determine whether there is a mismatch between the return address 353 provided by the speculative CALL/RET stack 406 at block 2014 and the return address 355 provided by the non-speculative CALL/RET stack 414 at block 2026, as described above with respect to Figure 4 and block 1324 of Figure 13. If so, flow proceeds to block 2034; otherwise, flow ends.

At block 2034, the control logic 404 controls the mux 422 to cause fetching to branch to the return address 355 provided by the non-speculative CALL/RET stack 414 at block 2026, as described above with respect to Figure 4 and block 1326 of Figure 13. Flow ends at block 2034.